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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,183	MATSUO, MIE	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 4-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 3/19/2007, with respect to the rejection(s) of claim(s) 2, 7, and 9 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below in view of the Siniaguine and Swan references.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 14, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (U.S. PG Pub #2002/0084513), in view of Mikawa et al (U.S. PG Pub #20020115226).

With respect to **claim 2**, Siniaguine teaches a semiconductor substrate (Fig. 5, 110); a plurality of source/drain regions on the substrate (Fig. 5, 204); and a through plug formed to have a side surface being in contact with the diffusion layer patterns (Fig. 5, through plug comprising 140/150/160), the side surface being surrounded by the diffusion layer patterns without being in contact with the insulation film (Fig. 5, layer 140 is in contact with source/drain 204), and to pass through the diffusion layer patterns and the semiconductor substrate; but

does not teach that the source/drain regions are formed of a plurality of diffusion layer patterns formed on the semiconductor substrate; an insulation film formed between the diffusion layer patterns on the semiconductor substrate.

Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12), and furthermore that the insulation film is formed to isolate the plural diffusion layer patterns from one another, as set forth in **claim 21**. It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor substrate of Siniaguine with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the diffusion layer pattern, in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

With respect to **claim 14**, Siniaguine teaches that the through plug has a columnar electric conductor made of copper (Fig. 5, 150 and Paragraph 26), and an insulation layer made of any one of silicon oxide, silicon nitride, and a combination of silicon oxide and silicon nitride, the insulation layer surrounding the columnar electric conductor (Paragraph 14).

With respect to **claim 22**, Siniaguine does not teach diffusion layer patterns are dummy diffusion layer patterns. Mikawa teaches diffusion layer patterns that are dummy diffusion layer patterns (Paragraph 50, Cell B). It would

have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Siniaguine with a dummy diffusion pattern based on the teachings of Mikawa in order to create a dummy cell in the memory area.

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine and Mikawa, in view of Mashino et al (2002/0190375).

With respect to **claims 5 and 8**, Siniaguine does not teach a pattern portion formed above the diffusion layer patterns and/or the insulation film without being in contact with the through plug; the pattern portion uses a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta). Mashino teaches a pattern portion formed above the semiconductor element formation layer comprising copper wherein the through plug is partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 205b and Paragraph 117). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper as the metallization layer of Swan as taught by Mashino because copper has been shown to be a suitable material for this purpose.

Claims 4, 6, 7, 9, 13, 15, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swan et al (U.S. PG Pub #2003/0210534), in view of Mikawa et al (U.S. PG Pub #2002/0115226), further in view of Mashino et al (U.S. PG Pub #2002/0190375).

With respect to **claims 4 and 7**, Swan teaches a semiconductor substrate (Fig. 5, 12); a plurality of transistors formed on the semiconductor substrate (Fig. 5, 24); an insulation film formed between the transistors on the semiconductor substrate to isolate the transistors from one another (Fig. 5, 32); a pattern portion formed above the diffusion layer patterns and/or the insulation film (Fig. 5, 34), and a through plug formed to have a side surface being in contact with the insulation film (Fig. 5, through plug comprising 48/62/64), the side surface being surrounded by the insulation film without being in contact with the transistors, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded also by the pattern portion above the transistors and/or the insulation film and being insulated from the pattern portion; but does not teach that the transistor is formed by diffusion layer patterns with an insulation film formed between the diffusion layer patterns; or that the pattern portion uses a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta).

Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor substrate of Siniaguine with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the diffusion layer pattern, in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

Mashino teaches a pattern portion formed above the semiconductor element formation layer comprising copper wherein the through plug is partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 205b and Paragraph 117). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper as the metallization layer of Swan as taught by Mashino because copper has been shown to be a suitable material for this purpose.

With respect to **claims 6 and 9**, Swan teaches a plurality of semiconductor chips (Fig. 6, 10 and 110), at least one of the semiconductor chips including: a semiconductor substrate (Fig. 5, 12); a plurality of transistors formed on the semiconductor substrate (Fig. 5, 24); an insulation film formed between the transistors on the semiconductor substrate to isolate the transistors from one another (Fig. 5, 32); a pattern portion formed above the diffusion layer

patterns and/or the insulation film (Fig. 5, 34), and a through plug formed to have a side surface being in contact with the insulation film (Fig. 5, through plug comprising 48/62/64), the side surface being surrounded by the insulation film without being in contact with the transistors, and to pass through the insulation film and the semiconductor substrate, the through plug being partly surrounded also by the pattern portion above the transistors and/or the insulation film and being insulated from the pattern portion; a connecting member electrically connecting the through plugs of the at least one of the semiconductor chips to at least one of the semiconductor chips (Figs. 5 and 6, 70); but does not teach that the transistor is formed by diffusion layer patterns with an insulation film formed between the diffusion layer patterns; or that the pattern portion uses a material thereof one kind selected from a group consisting of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), tantalum (Ta), and a chemical compound composed of at least one metal out of aluminum (Al), tungsten (W), titanium (Ti), copper (Cu), and tantalum (Ta).

Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor substrate of Siniaguine with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the

diffusion layer pattern, in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

Mashino teaches a pattern portion formed above the semiconductor element formation layer comprising copper wherein the through plug is partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 205b and Paragraph 117). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper as the metallization layer of Swan as taught by Mashino because copper has been shown to be a suitable material for this purpose.

With respect to **claims 13 and 15**, Swan teaches that the through plug has a columnar electric conductor made of copper (Paragraph 23), and an insulation layer made of any one of silicon oxide, silicon nitride, and a combination of silicon oxide and silicon nitride, the insulation layer surrounding the columnar electric conductor (Paragraph 21).

With respect to **claims 23 and 24**, Swan does not teach diffusion layer patterns are dummy diffusion layer patterns. Mikawa teaches diffusion layer patterns that are dummy diffusion layer patterns (Paragraph 50, Cell B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Swan with a dummy diffusion pattern based on the teachings of Mikawa in order to create a dummy cell in the memory area.

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swan, Mikawa, and Mashino, further in view of Mayashita et al (U.S. PG Pub #2001045605).

With respect to **claim 10**, Swan does not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Swan and Mikawa in order to decrease the parasitic resistance of the device.

With respect to **claim 12**, Swan does not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Swan and Mikawa in order to decrease the parasitic resistance of the device.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine and Mikawa, in view of Mayashita.

With respect to **claim 11**, Siniaguine and Mikawa do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a

diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine/Swan, Mikawa, and Mashino, in view of Sakao (U.S. Patent #6166425).

With respect to **claims 16 and 18-20**, Swan teaches that a diameter of the through plug is 25 to 50 micrometers (Paragraph 20), but does not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Swan and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Swan based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 17**, Siniaguine teaches that a diameter of the through plug is greater than 1 micrometer (Paragraphs 14 and 16), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a

semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Siniaguine and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Siniaguine based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

EVAN PERT
PRIMARY EXAMINER